Amendments to the Specification:

Please replace the Title with the following amended Title:

-- Integrated Semiconductor Memory with a Selection Transistor Formed at a [[Web]]Ridge--.

Please replace the paragraph at page 1, beginning on line 2, with the following amended paragraph:

This application claims priority under 35 USC §119 to German Application No. 10256973.8, filed on December 5, 2002, and titled "Integrated Semiconductor Memory With A Selection Transistor Formed at a [[Web]] Ridge," the entire contents of which are hereby incorporated by reference.

Please replace the paragraph at page 2, beginning on line 4, with the following amended paragraph:

One design of the selection transistor in the memory region is the surrounding gate transistor. [[Webs]] Ridges made of substrate material formed by a perpendicular etching are used as a basic structure for the formation of the transistor. In this case, the patterned, usually elongate, [[web]] ridge is covered with a gate dielectric and surrounded from all sides, except for the top side, with a peripheral gate electrode formed by a spacer technique. A trench capacitor is arranged at one end of the [[web]] ridge. A first, lower source/drain region is formed by outdiffusion from the inner capacitor electrode of the trench capacitor. On the top side of the [[web]] ridge, a second, upper source/drain region is implanted so that a vertical selection transistor is produced at one lateral end of the [[web]] ridge at which the trench capacitor is

situated. Alternatively, the vertical selection transistors can be formed in the interior of a capacitor trench above the storage capacitor.

Please replace the paragraph at page 2, beginning on line 14, with the following amended paragraph:

Furthermore, there are semiconductor memories with planar selection transistors in the memory cell array, which are arranged laterally with respect to the connected storage capacitors. These selection transistors do not have a [[web]] ridge made of substrate material.

Please replace the paragraph at page 3, beginning on line 10, with the following amended paragraph.

An integrated semiconductor memory can be operated with a higher current for writing in and/or reading out information and which can be less susceptible to leakage currents. Generally, an integrated semiconductor including a [[web]] ridge arranged on an insulation layer, a first source/drain region arranged on the insulation layer at one lateral end of the [[web]] ridge, and a second source/drain region is arranged on the insulation layer at another lateral end of the [[web]] ridge. Also, the two longitudinal sides of the [[web]] ridge and a top side of the [[web]] ridge can be covered with a layer sequence comprising a gate dielectric and a gate electrode.

Please amend the paragraph beginning at page 3, line 17 and ending at page 4, line 4, with the following amended paragraph.

A memory cell in a memory cell array can include a transistor in which the transistor channel's current flow direction can run parallel to the insulation layer. The transistor can be

provided at a [[web]] ridge made of substrate material. The current flow direction can also parallel the longitudinal direction of the [[web]] ridge. Both longitudinal sides and the top side of the [[web]] ridge can be covered by a gate dielectric and a gate electrode can be arranged above the gate dielectric. This can result in a significantly larger channel width than in conventional selection transistors, since twice the [[web]] height of the ridge (in each case at the left-hand and right-hand longitudinal side of the [[web]] ridge) and the [[web]] width of the ridge together produce the channel width. Consequently, by large [[web]] ridge heights, without enlarging the basic area of the memory cell, it is possible to achieve high channel widths, i.e., high currents for storing and reading out information, as a result of which the write and read speed of the semiconductor memory can increase.

Please replace the paragraph at beginning at page 5, line 4, with the following amended paragraph.

In the case without a collar region, by contrast, the storage capacitor can be formed as far as the buried insulation layer arranged directly below the [[web]] ridge, as a result of which its capacitance rises.

Please replace the paragraph at beginning at page 5, line 13, with the following amended paragraph.

The top side of the surface contact can be arranged below the level of the top side of the [[web]] ridge and cab be electrically insulated from a word line passing the storage capacitor by an insulating upper filling structure. This word line (passing word line) can be formed at the same level as the word line, which can be connected to the selection transistor and can cover the

top side of the [[web]] ridge. The passing word line running at the same level can be insulated from the top side of the upwardly shortened surface contact by the upper filling structure.

Please replace the paragraph beginning at page 6, line 1 with the following amended paragraph:

The second source/drain region can have, in the longitudinal direction of the web ridge, the same dimension, i.e., the same width, as the underside of a spacer of a word line covering the [[web]] ridge. The second source/drain region can be connected to a bit line contact on the side remote from the web. Consequently, one of the source/drain regions can be with the aid of the word line spacer. That side area of the source/drain region which is remote from the [[web]] capacitor may be connected by a bit line contact 17a to a bit line running above the [[web]] ridge and above the word line.

Please replace the paragraph beginning at page 6, line 7, with the following amended paragraph:

Accordingly, a bit line can be arranged above the [[web]] ridge, can run parallel to the longitudinal direction of the [[web]] ridge, and can be connected to the second source/drain region. By this bit line, [[webs]] ridges, which can be strung together in their longitudinal direction and can be interrupted by capacitor trenches, may be contact-connected at a respective end via the bit line contact. In the direction of the word lines adjacent to the [[webs]] ridges and at a level below the bit lines, provided that no word lines run there, the memory cell array can be filled with an insulating material, for example, an oxide or nitride.

Please replace the paragraph beginning at page 6, line 14, with the following amended paragraph:

A word line can run perpendicular to the longitudinal direction of the [[web]] ridge, and can cover the gate dielectric on both longitudinal sides and on the top side of the [[web]] ridge. The gate electrode that is formed by the word line and is isolated from the semiconductor material of the [[web]] ridge only by the gate oxide layer at both side walls of the [[web]] ridge which run in the longitudinal direction, leads to a channel width which is only limited by the [[web]] height of the ridge. The channel width can thus be chosen to be larger than the structure width (critical dimension), i.e., the optical resolution limit used in the lithographic patterning. The [[web]] ridge may be patterned in a manner narrower than the optical resolution limit. For example, it may be narrower than the bit line running above it. The channel width is not appreciably impaired thereby, since essentially the [[web]] ridge height contributes to the channel width.

Please replace the paragraph beginning at page 7, line 1, with the following amended paragraph:

The semiconductor memory can have a multiplicity of memory cells of the semiconductor memory with selection transistors formed at [[webs]] ridges, a bit line contact being arranged only at every second crossover point between a bit line and a word line and a word line passing above or below a storage capacitor at the remaining crossover points. The selection transistors formed at the [[webs]] ridges can thus be arranged relative to the direction of the word lines and bit lines in a diagonal grid of selection transistors that are the most closely adjacent to one another.

Please replace the paragraph beginning at page 7, line 21 and ending at page 8, line 9, with the following amended paragraph:

FIG. 1 shows an integrated semiconductor memory 10 with an SOI substrate 20. The buried insulation layer 11 can be arranged directly below the selection transistors 3 of the memory cells 1. The selection transistors can be formed at [[webs]] ridges 4. The buried insulation layer, preferably oxide layer 11, can have openings in which a trench capacitor 2 can be incorporated into the substrate 20 and can be connected to a first source/drain region 5 of the selection transistor 3 by a contact arranged in the opening, a surface contact 19. The first source/drain region 5 can be situated at a first end A of the [[web]] 4 running in the longitudinal direction x, and the second source/drain region 6 can be arranged at the other lateral end B of the [[web]] ridge. The [[web]] ridge can extend between the ends A, B with its main extending direction x, which can coincide with the current flow direction I of the transistor channel, and can be surrounded from above and also on its side walls above and below the plane of the drawing by a gate oxide 9 and a gate layer sequence 16.

Please replace the paragraph beginning at page 8, line 14, with the following amended paragraph:

FIG. 2 is a cross-sectional view, taken along the line C-C of FIG. 1, i.e., perpendicular to the plane of the drawing of FIG. 1. In FIG. 2, the transistor channel runs perpendicularly to the plane of the drawing through the [[web]] ridge, along the two side areas 14 and along the top side 15. There, the gate layer sequence 16, can be composed, for example, of a lower gate layer 7, for instance, made of polysilicon, and an upper gate layer, which may contain tungsten, can be

isolated from the channel region of the [[web]] ridge 4 only by the gate oxide 9 or some other dielectric.

Please replace the paragraph beginning at page 8, line 20, with the following amended paragraph:

The dimensions in FIG. 2 are not illustrated to scale. The [[web]] height of the ridge can be greater than the optical resolution limit used in the lithographic exposure during the fabrication of the semiconductor memory. In particular, the [[web]] ridge height and thus the height of the side areas 14 may be greater than the distance between the bit lines 17, thus resulting in a larger channel width than in the case of a conventional selection transistor. In FIG. 2, the oxide layer 11 can be arranged below the [[web]] ridge and the bulk material of the substrate 20, which can be doped, in particular, heavily n-doped, can be arranged below the oxide layer. Alternatively, the doping of the [[web]] ridge 4 may be adapted to the desired electrical properties of the selection transistor. In particular, the semiconductor material of the [[web]] ridge 4 may be doped with a different doping type, a different dopant and/or a different dopant concentration than the semiconductor material 20 below the buried oxide layer 11. In FIG. 2, the bit line 17 can be insulated from the word line 16 by an oxide layer 22 or a different dielectric.

Please replace the paragraph beginning at page 9, line 9, with the following amended paragraph:

The [[web]] ridge 4, illustrated in cross section perpendicular to the current direction in FIG. 2, can run from right to left between the first and second source/drain regions 5, 6 in FIG. 1.

The surface contact 19 can have a top side arranged at a deeper level than the top side 15 of the [[web]] ridge 4 and may therefore readily be covered by an insulating filling structure 30, for example, an oxide, before a passing word line 16a can be deposited above the capacitor trench. An insulation layer 22 can be deposited in order to insulate the word lines from the bit lines.

Please replace the paragraph beginning at page 10, line 4, with the following amended paragraph:

FIG. 3 shows, in plan view, an arrangement of seven storage capacitors 2, which are connected toward the right-hand side to a respective selection transistor 3 formed in each case at a [[web]] ridge 4. The storage capacitors 2 can be arranged below the buried insulation layer 11, whereas the selection transistors 3 can be arranged above the buried insulation layer 11. The word lines 16 can cross the longitudinal direction x of the [[webs]] ridges 4 and can cover both longitudinal sides and the top side of the [[webs]] ridges. As a result, a large channel width can be obtained. By using narrow [[webs]] ridges which may be configured narrower in direction y, with the aid of spacers, than the distance between the bit lines 17, charge carriers in the semiconductor material of the [[web]] ridge can be depicted, so that an ideal on/off current characteristic of the selection transistor 3 can be achieved. The subthreshold transconductance of such a transistor can be higher than a conventional transistor. A higher current can be achieved with a significantly reduced voltage at the gate. This affords advantages over conventional memory types, for instance, a higher current consumption and a smaller area taken by the circuits.

Please replace the paragraph beginning at page 10, line 17, with the following amended paragraph:

In FIG. 3, the [[webs]] ridges can be arranged in rows along the bit lines 17 running above them. Adjacent [[webs]] ridges 4 in direction y of the word lines 16 can be offset with respect to one another in the x direction, so that such adjacent memory cells, which can be driven by two different word lines 16, can be simultaneously connected by two different bit lines 17.

Please replace the paragraph beginning at page 11, line 3, with the following amended paragraph:

The photolithographic etching of the capacitor trenches can be followed by the deposition of the capacitor dielectric (for instance, a nitride, oxide, an aluminum oxide, etc.) and, on the latter, the inner capacitor electrode can be made, for example, of heavily n-doped polysilicon. The material of the inner capacitor electrode can be etched back at most as far as the lower edge of the buried insulation layer 11 of the semiconductor substrate 20. The capacitor dielectric 13 can then be removed at the level of the [[web]] ridge.

Please replace the paragraph beginning at page 11, line 9, with the following amended paragraph:

A polysilicon layer can be deposited and subsequently etched back approximately as far as the level of the top side of the [[web]] ridge or a little deeper. Half of each surface contact 19 can be removed in the direction of its nearest left-hand [[web]] ridge 4. The resulting opening can be filled with an insulating material, for instance, an oxide 30, which can also cover the top side of the surface contact 19.

Please replace the paragraph beginning at page 11, line 14, with the following amended paragraph:

Afterward, a hard mask for patterning the [[webs]] ridges can be patterned lithographically. In order to fabricate particularly fine hard mask structures for patterning the webs, a spacer can be used as mask. As a result, [[web]] ridge widths in the y direction can be narrower than the lithographic resolution limit, which can be used for patterning and with which word lines and bit lines can be patterned. After etching of the surroundings of the [[webs]] ridges, the etching mask can be removed, doping of the channel region can be introduced by implantation into the semiconductor material of the web, and a gate oxide layer can be grown.

Please replace the paragraph beginning at page 12, line 12, with the following amended paragraph:

Finally, a metal can be deposited for fabricating the bit line contacts 17a and the bit lines themselves. In this way, a selection transistor with a transistor channel having a horizontal current direction can be fabricated at the [[webs]] ridges in the memory cell array, which selection transistor, in the on state, can enable a high write and read current to the storage capacitor 2 and, in the off state, can be insulated from the material of the semiconductor substrate 20 by the buried insulation layer 11.

Please replace the paragraph beginning at page 14, line 1, with the following amended paragraph:

1 Memory cell

2	Storage capacitor
3	Selection transistor
4	[[Web]] Ridge
5	First source/drain region
6	Second source/drain region
7	Lower gate layer
8	Upper gate layer
9	Gate dielectric
10	Integrated semiconductor memory
11	Buried insulation layer
12	Inner capacitor electrode
13	Capacitor dielectric
14	Longitudinal side of a [[web]] ridge
15	Top side of a [[web]] ridge
16	Gate electrode
17	Bit line
18	Inner wall of a storage capacitor
19	Surface contact
20	Semiconductor substrate
21	Spacer
22	Oxide layer
23	Nitride layer
24	Further spacer
25	Insulating filling
26	Bottom of the storage capacitor
30	Insulating filling structure
A, B	Lateral [[web]] ridge ends
I	Current flow direction of the transistor channel